Abinash Mohanty

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Summary

Passionate programmer with doctorate degree in deep learning and 5+ years of industry experience. Rich hands-on experience in end-to-end deep learning developement comprising of dataset generation, network design and training for high inference accuracy and SoC architecture exploration and implementation with hardware accelerators (silicon proven ASIC and FPGA). Single handedly implemented the complete software framework from scratch for (1) compiling and mapping networks, described in high level frameworks like tensorflow and caffe, to hardware accelerator,(2) creating, training and testing neural networks, and (3) providing golden outputs for hardware validation team.

Technical Skills

- Languages: Python, Verilog, C++, MATLAB, OpenCL
- Tools and Frameworks: TensorFlow, Caffe, Xilinx and Altera High Level Synthesis
- Trainings: IBM TrueNorth BootCamp (deep learning on IBM Synapse), Altera OpenCL Optimization

Professional Experience

- **FABU Tech, Tempe, AZ** *Aug, 2018 – Present (6 months)*
  Senior Design Engineer **(one of first 5 employees)**
  - Single handedly implemented the complete software framework with tensorflow and caffe backend.
  - Designed & trained neural networks for object detection and lane tracking for autonomous driving.

- **MobAI Tech Inc, Tempe, AZ** *May, 2018 – Aug, 2018 (3 months)*
  Deep Learning Research Intern
  - Conceptualized and implemented a novel NMS algorithm (without sorting & complexity of O(n)).
  - Implemented ASIC for fast NMS with novel O(1) insertion & deletion hardware lists (*patent submitted*).

- **MobAI Tech Inc, Tempe, AZ** *Dec, 2017 – May, 2018 (6 months)*
  Deep Learning Consultant
  - Deep learning for computer vision (object detection, lane tracking, traffic light detection).
  - Explored the architecture for SoC system and programmable deep learning accelerator.

- **Boehringer Ingelheim, Germany** *June, 2017 – July, 2017 (1 month)*
  Deep Learning Consultant
  - Conceptualized and developed the full stack including dataset generation, pre-processing, network architecture & training for a small footprint neural network to detect cough in raw audio.

- **Intel Corporation, Santa Clara, CA** *May, 2016 – Oct, 2016 (5 months)*
  Graduate Intern
  - System level modeling & performance benchmarking of hardware accelerator for speech processing.
  - Conceptualized a novel memory architecture for efficient online training *(patent submitted)*.

- **Samsung Research Institute, Noida, India** *June, 2010 – July, 2013 (3 years)*
  Senior Software Engineer II
  - Developed embedded application platform with stereoscopic 3D graphics rendering capabilities.
  - Implemented NPAPI Plugins & JavaScript Engine for running applications on smart televisions.

Academic Qualifications

- **Arizona State University, USA** *CGPA: 3.86/4.00*
  Doctor of Philosophy in Electrical Engineering *Aug. 2013 – Oct. 2018*

- **National Institute of Technology, India** *CGPA: 8.18/10.0*
  Bachelor of Technology in Electronics & Comm. Engineering *May 2006 – May 2010*

Key Academic and Research Projects

- **Automatic Cough Detection using Deep Neural Networks**
  - Designed & trained deep neural networks to detect coughs in raw audio recorded using VitaloJAK wearable microphone.
  - Achived **state-of-the-art** average leave-one-out cross-validation specificity(93.7%) and sensitivity (97.6%).

- **Network Growth & Transfer Learning for Inference using Non-ideal Hardware Accelerators**
  - Developed a bifurcated network growth technique to finetune pre-trained parameters & compensate for device variations.
  - Demonstrated $30\times \sim 100\times$ speed improvements with deep networks compared to existing methodologies.

- **Hardware Acceleration of Deep Convolutional Neural Networks for Machine Learning.**
  - Analyzed operation of deep networks & modified the layers to improve efficiency & optimize from hardware point of view.
  - Implemented a heterogenous system for acceleration with low-precision FPGA accelerator achiveing 68.3 GOPS.

- **Real-time Face Detection with Cascaded Random Forests using Custom Hardware Accelerator**
  - Designed a cascaded week classifier optimized for hardware acceleration ($30\times \sim 1000\times$ performance improvement).
  - Successfully taped-out & demonstrated realtime face & traffic signs detection with accelerators on ASIC & FPGAs.

- **Parallel architecture with resistive cross-point array for online dictionary learning.**
  - Conceptualized a hardware architecture using cross-point arrays of RRAM devices targeted towards learning algorithms.
  - Designed & implemented peripheral circuits necessary for dictionary update operations needed for online learning.

Relevant Publications

- **Mohanty, A.**, Du, X., Chen, P., Seo, J.S., Yu, S., Cao, Y., "Random Sparse Adaptation for Accurate Inference with Inaccurate Multi-level RRAM Arrays," in *IEEE International Electron Devices Meeting (IEDM),* 2017 .

- Kadambi, P., **Mohanty, A.**, Ren, H., Smith, J., McGuinnes, K., Holt, K., Furtwaengler, A., Slepetys, R., Yang, Zheng., Seo, J.S., Vrudhula, S., Chae, J., Cao, Y., Berisha, V., "Towards a wearable cough detector based on deep neural networks," in *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP),* 2017.

- **Mohanty, A.**, Suda, N., Kim, M., Vrudhula, S., Seo, J. S., and Cao, Y., "High-performance face detection with CPU-FPGA acceleration," in *IEEE International Symposium Circuits and Systems (ISCAS),* 2016, pp. 117-120.

- Kim, M., **Mohanty, A.**, Kadetotad, D., Suda, N., Wei, L., Saseendran, P., He, X., Cao, Y. and Seo, J.S., "A real-time 17-scale object detection accelerator with adaptive 2000-stage classification in 65nm CMOS," in *Design Automation Conference (ASP-DAC), 2017 22nd Asia and South Pacific,* 2017, pp. 21-22.

- Suda, N., Chandra, V., Dasika, G., **Mohanty, A.**, Ma, Y., Vrudhula, S., Seo, J.S. and Cao, Y., "Throughput-optimized OpenCL-based FPGA accelerator for large-scale convolutional neural networks," in *Proceedings of the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA),* 2016, pp. 16-25.

- Du, X., Krishnan, G., **Mohanty, A.**, Zheng Li, Charan, G., Cao, Y., "Towards Efficient Neural Networks On-A-Chip: Joint Hhardware-Algorithm Approaches," in *China Semiconductor Technology International Conference (CSTIC),* 2019, *Invited*

- Kim, M., **Mohanty, A.**, Kadetotad, D., Wei, L., He, X., Cao, Y. and Seo, J.S., "A real-time 17-scale object detection accelerator with adaptive 2000-stage classification in 65nm CMOS," in *Transactions on Circuits and Systems (TCAS)* 2019 *Submitted*

- **Mohanty, A.**, Sutaria, K., Awano, H., Sato, T., and Cao, Y., "RTN in Scaled Transistors for On-chip Random Seed Generation," in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI),* 2017 Apr 12.

- Xu, Z., **Mohanty, A.**, Chen, P.Y., Kadetotad, D., Lin, B., Ye, J., Vrudhula, S., Yu, S., Seo, J.S. and Cao, Y., "Parallel programming of resistive cross-point array for synaptic plasticity," in *BioTL,* 2014, pp.126-133.

- Kadetotad, D., Xu, Z., **Mohanty, A.**, Chen, P.Y., Lin, B., Ye, J., Vrudhula, S., Yu, S., Cao, Y. and Seo, J.S., "Parallel architecture with resistive crosspoint array for dictionary learning acceleration," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* 2015, pp.194-204.

- Chen, P.Y., Kadetotad, D., Xu, Z., **Mohanty, A.**, Lin, B., Ye, J., Vrudhula, S., Seo, J.S., Cao, Y. and Yu, S., "Technology-design co-optimization of resistive cross-point array for accelerating learning algorithms on chip," in *Design, Automation & Test in Europe Conference and Exhibition (DATE),* 2015, pp. 854-859.

- Kadetotad, D., Xu, Z., **Mohanty, A.**, Chen, P.Y., Lin, B., Ye, J., Vrudhula, S., Yu, S., Cao, Y. and Seo, J.S., "Neurophysics-inspired parallel architecture with resistive crosspoint array for dictionary learning," in *Biomedical Circuits and Systems Conference (BioCAS),* 2014, pp. 536-539.

- Seo, J.S., Lin, B., Kim, M., Chen, P.Y., Kadetotad, D., Xu, Z., **Mohanty, A.**, Vrudhula, S., Yu, S., Ye, J. and Cao, Y., "On-chip sparse learning acceleration with CMOS and resistive synaptic devices," in *IEEE Transactions on Nanotechnology (TNANO),* 2015, pp.969-979.